REMARKS

Applicants respectfully request consideration of the following remarks.

Obviousness Rejections Under 35 U.S.C. § 103

To reject a claim or claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. M.P.E.P. § 2142. When establishing a prima facie case of obviousness, the Examiner must set forth evidence showing that the following three criteria are satisfied:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references (or references when combined) must teach or suggest all the claim limitations. M.P.E.P. § 2143.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on the applicant's disclosure. M.P.E.P. § 2142 (citing *In re Vaeck*, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991)). Also, the evidentiary showing of a motivation or suggestion to combine prior art references "must be clear and particular." *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999).

Obviousness Rejection Based on U.S. Patent 6,772,189 to Asselin in View of U.S. Patent 6,470,397 to Shah et al.

Claims 1, 2, 5-8, 10-16, 18-21, 24-27, and 29-35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,772,189 to Asselin (hereinafter "Asselin") in view of U.S. Patent 6,470,397 to Shah et al. (hereinafter "Shah"). Applicants respectfully traverse this rejection, as set forth below.

Independent claim 1 recites:

> 1. A computer implemented method comprising:
>
> requesting a first deferred procedure call for a first interrupt event associated with a source;
>
> requesting at least one other ***different*** deferred procedure call for a second interrupt event associated with the source, wherein the first interrupt event comprises one type of event and the second interrupt event comprises another type of event;
>
> assigning the first deferred procedure call and the at least one other deferred procedure call to a resource;
>
> **processing the first interrupt event with the first deferred procedure call**; and
>
> **processing the second interrupt event with the at least one other deferred procedure call**.

Each of independent claims 8, 20, and 27 recites some limitations similar to those recited in claim 1.

Independent claim 12, as amended, recites:

> 12. A driver comprising:
> an interrupt handler to identify interrupt events associated with a source;
> a first deferred procedure call, **the first deferred procedure call to process a first type of the interrupt events**; and
> a second ***different*** deferred procedure call, **the second deferred procedure call to process a second type of the interrupt events**.

Independent claim 15, as amended, recites some limitations similar to those recited in claim 12.

Referring, for example, to claim 1 above, one embodiment of the claimed invention is directed to a method for handling multiple interrupt events using at least two different deferred procedure calls, each of the two deferred procedure calls corresponding to a certain type of interrupt event. Similarly, referring to claim 12 above, one embodiment of the claimed invention is directed to a driver including two different deferred procedure calls, each of the deferred procedure calls corresponding to a certain type of interrupt event.

As noted by the Examiner, "Asselin does not specifically teach processing each interrupt event with a different deferred procedure call." Office Action, at pg. 4. To overcome the lack of disclosure in Asselin, the Examiner relies upon Shah, stating:

> Shah teaches a driver architecture supported by a variety of routines, including a interrupt DPC routine [col. 9, lines 16-23] and processing each interrupt event with a different deferred procedure call [**list of tasks which may be performed by the interrupt DPC routine** . . . e.g. Upon detection of fatal error, the DPC routine returns all commands and reinitializes adapter. Upon detection of bus reset, the DPC routine cleans up queued commands, restarts the host adapter

queue, and notifies other connected drivers; col 12, line 51 – col. 13, lines 30]. Office Action, at pg. 4 (emphasis added).

Shah does not disclose the use of different interrupt DPCs to process alternate types of interrupt events but, rather, Shah discloses the use of the **same** interrupt DPC to handle a number of different tasks. See, e.g., Shah at column 12, line 51 through column 13, line 27, and in particular, refer to column 12, lines 57-58, where it is stated: "The following is an exemplary list of tasks which may be performed by **the** interrupt DPC routine." Further, the Examiner expressly states that Shah discloses a "list of tasks which may be performed by **the** interrupt DPC routine", as noted in the passage above. In sum, Shah does not disclose the use of different DPCs to handle alternate types of interrupt events, and the Examiner has not identified any specific text or teaching in this reference to the contrary.

As Asselin and Shah, either individually or in combination, fail to disclose at least the above-noted limitations of independent claims 1, 8, 12, 15, 20, and 27, each of these claims is nonobvious in view of these references. Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. §2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 2, 5, 6, 7, and 31 are allowable as depending from nonobvious independent claim 1, claim 10, 11 and 32 are allowable as depending from nonobvious independent claim 8, claims 13, 14, and 33 are allowable as depending from nonobvious independent claim 12, claims 16, 18 and 19 are allowable as depending from nonobvious independent claim 15, claims 21, 24, 25, 26, and 34 are allowable as depending from nonobvious independent

claim 20, and claims 29, 30, and 25 are allowable as depending from nonobvious independent claim 27.

Obviousness Rejection Based on U.S. Patent 6,772,189 to Asselin in View of U.S. Patent 6,470,397 to Shah et al. and Further in View of U.S. Patent 6,378,004 to Galloway et al.

Claims 3, 4, 9, 17, 22, 23, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Asselin in view of Shah and further in view of U.S. Patent 6,378,004 to Galloway (hereinafter "Galloway"). Applicants respectfully traverse this rejection, as set forth below.

As previously set forth, Asselin and Shah, either individually or in combination, fail to disclose at least the above-noted limitations of each of independent claims 1, 8, 15, 20, and 27, and Galloway also fails to disclose these limitations. Thus, Asselin, Shah, and Galloway, either individually or in combination, fail to disclose at least the above-noted limitations of independent claims 1, 8, 15, 20, and 27, and these claims are non-obvious in view of these references. If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. §2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 3-4, 9, 17, 22-23, and 28 are allowable as depending from nonobvious, independent claims 1, 8, 15, 20, and 27, respectively.

CONCLUSION

Applicants submit that claims 1-35 are in condition for allowance and respectfully requests allowance of such claims.

Please charge any shortages and credit any overages to Deposit Account No. 02-2666.

Respectfully submitted,

Date: November 4, 2005

/Kerry D. Tweet/
Kerry D. Tweet, Reg. No. 45,959

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(503) 684-6200

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail on the below date with sufficient postage in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

Signature: Theresa Belland 11/4/05
Theresa Belland Date